WHAT IS CLAIMED IS:

1. A tuner circuit comprising:

an input terminal;

an input tuning circuit for tuning to an RF signal of a desired channel among RF signals of a plurality of channels input from the input terminal;

a variable-gain amplifier circuit for amplifying or attenuating a level of an RF signal output from the input tuning circuit to a prescribed level;

a pre-amplifier circuit disposed at an upstream side of the input tuning circuit; and

a variable attenuator circuit disposed at an upstream side of the pre-amplifier circuit, including a PIN diode disposed in series with a signal path of the tuner circuit, the PIN diode having characteristics between direct current and intermodulation distortion such that intermodulation distortion of a signal that flows therethrough is maximized at a desired value of a direct current; wherein

the variable-gain amplifier circuit and the variable attenuator circuit are controlled according to a common AGC voltage that is set based on a level of an input RF signal, and operations of the variable-gain amplifier circuit and the variable attenuator circuit in relation to the AGC voltage are set such that when the input RF signal is at a maximum assumed level, a direct current that flows through the PIN diode is less than the predetermined value of a direct current that maximizes intermodulation distortion.

2. A tuner circuit according to Claim 1, wherein the operations of the variable-gain amplifier circuit and the variable attenuator circuit in relation to the AGC voltage are set such that the direct current that flows through the PIN diode is less than about 100 μA when the input RF signal is at the maximum assumed level.

3. A tuner circuit according to Claim 1, wherein the AGC voltage is initially set based on a signal level of a channel having the smallest gain at a signal-level detecting point.

4. A tuner circuit according to Claim 2, wherein the AGC voltage is initially set based on a signal level of a channel having the smallest gain at a signal-level detecting point.

5. A tuner circuit according to Claim 1, wherein the variable attenuator circuit includes at least three PIN diodes.

6. A tuner circuit according to Claim 5, wherein the at least three PIN diodes are arranged to constitute a π-shaped attenuation circuit.

7. A tuner circuit according to Claim 1, wherein the variable attenuator circuit includes a transistor, a choke coil, a plurality of resistors, and a plurality of capacitors.

8. A tuner circuit according to Claim 1, wherein a cathode of the PIN diode is connected to the input terminal.

9. A tuner circuit according to Claim 1, wherein an anode of the PIN diode is connected to an output terminal via at least one capacitor.

10. A tuner circuit according to Claim 7, wherein an anode of the PIN diode is connected to an emitter of the transistor via the choke coil.

11. A tuner circuit according to Claim 7, wherein the transistor is arranged such that a base of the transistor receives an AGC voltage input.